Listing of Claims:

1. (Previously Presented) A method comprising:

etching a source region and a drain region in a silicon substrate wherein the etching has an undercut profile;

depositing a silicon germanium alloy in the source region and in the drain region;

depositing nickel on the silicon germanium alloy;

forming a nickel silicon germanium silicide layer wherein the nickel silicon germanium silicide layer is self-aligned.

2. (Previously Presented) The method of claim 1 wherein the source region and the drain region extend laterally beneath an insulating layer.

3. (Previously Presented) The method of claim 2 wherein the source region and the drain region extend laterally beneath a gate region.

4. (Previously Presented) The method of claim 3 wherein the source region and the drain region extend laterally beneath the gate region between 25 and 200 angstroms.

5. (Previously Presented) The method of claim 1 wherein the source region and the drain region have a vertical depth between 100 and 1500 angstroms beneath the surface of the silicon substrate.

6. (Previously Presented) The method of claim 1 wherein the etching is dry SF_6-based.

7. (Previously Presented) The method of claim 1 wherein the silicon germanium alloy has a germanium composition between 5% and 50%.

8. (Previously Presented) The method of claim 7 wherein the silicon germanium alloy has a germanium composition between 10% and 40%.

9. (Previously Presented) The method of claim 8 wherein the silicon germanium alloy has a germanium composition between 15% and 30%.

10. (Previously Presented) The method of claim 1 wherein the deposition of the silicon germanium alloy is vapor phase epitaxy.

11. (Previously Presented) The method of claim 1 wherein the deposition of the silicon germanium alloy is reduced pressure chemical vapor deposition.

12. (Previously Presented) The method of claim 1 wherein the deposition of the silicon germanium alloy is atmospheric chemical vapor deposition.

13. (Previously Presented) The method of claim 1 wherein the deposition of the silicon germanium alloy is ultra high vacuum chemical vapor deposition.

14. (Previously Presented) The method of claim 1, depositing the silicon germanium alloy further comprising doping the alloy.

15. (Previously Presented) The method of claim 14 wherein the doping is in situ during depositing the silicon germanium alloy.

16. (Previously Presented) The method of claim 15 wherein a dopant is boron.

17. (Previously Presented) The method of claim 16 wherein a source of the dopant is B_2H_6.

18. (Previously Presented) The method of claim 16 wherein the boron has a doping concentration level between $1*10^{18}$ /cm^3 and $3*10^{21}$ /cm^3.

19. (Previously Presented) The method of claim 18 wherein the doping concentration level is $1*10^{21}$ /cm^3.

20. (Previously Presented) The method of claim 1 wherein the nickel has a thickness between 50 and 200 angstroms.

21. (Previously Presented) The method of claim 1, forming the nickel silicon germanium silicide layer further comprising:

annealing the substrate at a temperature between 325°C and 450°C for less than or equal to 60 seconds;

removing excess nickel with a wet etch chemistry of hot H_2O_2 and H_2SO_4; and

annealing the substrate at a temperature between 400°C and 550°

22. (Withdrawn) An transistor comprising:

a gate region;

an insulator region beneath the gate region;

a source region adjacent to the insulator region;

a drain region adjacent to the insulator region;

wherein the source region and the drain region include a silicon germanium alloy and a nickel silicon germanium silicide layer.

23. (Withdrawn) The method of claim 22 wherein the source region and the drain region extend laterally beneath the insulating layer.

24. (Withdrawn) The method of claim 23 wherein the source region and the drain region extend laterally beneath the gate region.

25. (Withdrawn) The method of claim 24 wherein the source region and the drain region extend laterally beneath the gate region between 25 and 200 angstroms.

26. (Withdrawn) The method of claim 22 wherein the source region and the drain region have a vertical depth between 100 and 1500 angstroms beneath the surface of a silicon substrate.

27. (Withdrawn) The transistor of claim 22 wherein the silicon germanium alloy has a germanium composition between 5% and 50%.

28. (Withdrawn) The transistor of claim 27 wherein the silicon germanium alloy has a germanium composition between 10% and 40%.

29. (Withdrawn) The transistor of claim 28 wherein the silicon germanium alloy has a germanium composition between 15% and 30%.

30. (Withdrawn) The transistor of claim 22 wherein the silicon germanium alloy is doped.

31. (Withdrawn) The transistor of claim 30 wherein the silicon germanium is doped in situ during a deposition of the silicon germanium alloy.

32. (Withdrawn) The transistor of claim 31 wherein a dopant is boron.

33. (Withdrawn) The transistor of claim 32 wherein a source of the dopant is B_2H_6.

34. (Withdrawn) The method of claim 32 wherein the boron has a doping concentration level between $1*10^{18}$ /cm^3 and $3*10^{21}$ /cm^3.

35. (Withdrawn) The method of claim 34 wherein the doping concentration level is $1*10^{21}$ /cm^3.

36. (Withdrawn) The transistor of claim 22 wherein the nickel silicon germanium silicide layer is self-aligned.

37. (Previously Presented) A method comprising:

etching a source region and a drain region in a silicon substrate wherein the etching has an undercut profile;

depositing a silicon germanium alloy in the source region and in the drain region wherein the silicon germanium alloy has a germanium composition between 15% and 30%;

doping the silicon germanium alloy in situ with boron wherein the boron has a doping concentration level of $1*10^{21}$ /cm^3;

depositing nickel on the silicon germanium alloy;

annealing the substrate at a temperature between 325°C and 450°C for less than or equal to 60 seconds;

removing excess nickel with a wet etch chemistry of hot H_2O_2 and H_2SO_4; and

annealing the substrate at a temperature between 400°C and 550°.

38. (Previously Presented) The method of claim 37 wherein the source region and the drain region extend laterally beneath an insulating layer.

39. (Previously Presented) The method of claim 38 wherein the source region and the drain region extend laterally beneath a gate region.

40. (Previously Presented) The method of claim 39 wherein the source region and the drain region extend laterally beneath the gate region between 25 and 200 angstroms.

41. (Previously Presented) The method of claim 37 wherein the source region and the drain region have a vertical depth between 100 and 1500 angstroms beneath the surface of the silicon substrate.

42. (Previously Presented) The method of claim 37 wherein the etching is dry SF_6-based.

43. (Previously Presented) The method of claim 37 wherein the deposition of the silicon germanium alloy is vapor phase epitaxy.

44. (Previously Presented) The method of claim 37 wherein the deposition of the silicon germanium alloy is reduced pressure chemical vapor deposition.

45. (Previously Presented) The method of claim 37 wherein the deposition of the silicon germanium alloy is atmospheric chemical vapor deposition.

46. (Previously Presented) The method of claim 37 wherein the deposition of the silicon germanium alloy is ultra high vacuum chemical vapor deposition.